FIG. 1
(PRIOR ART)

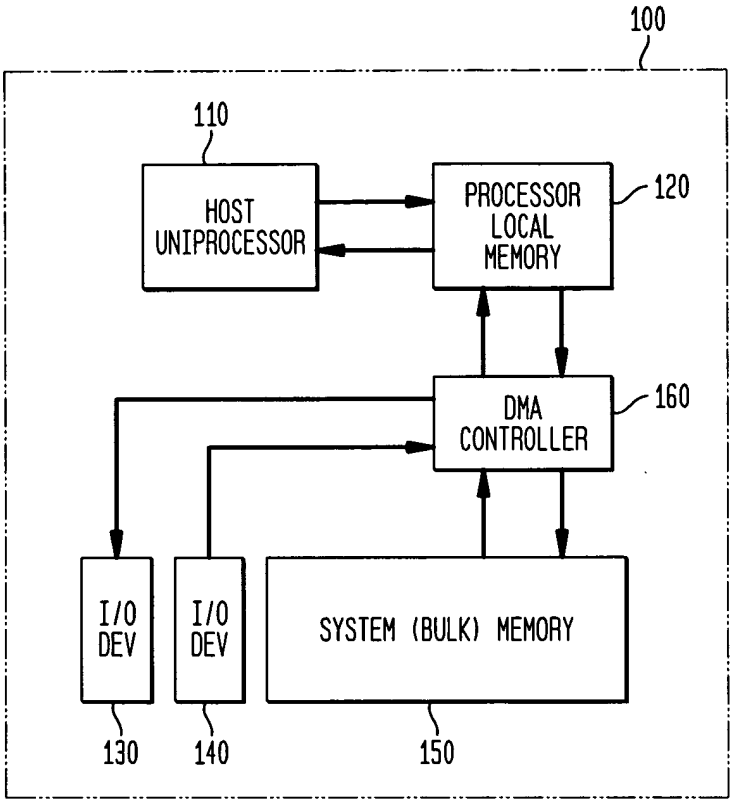


FIG. 2

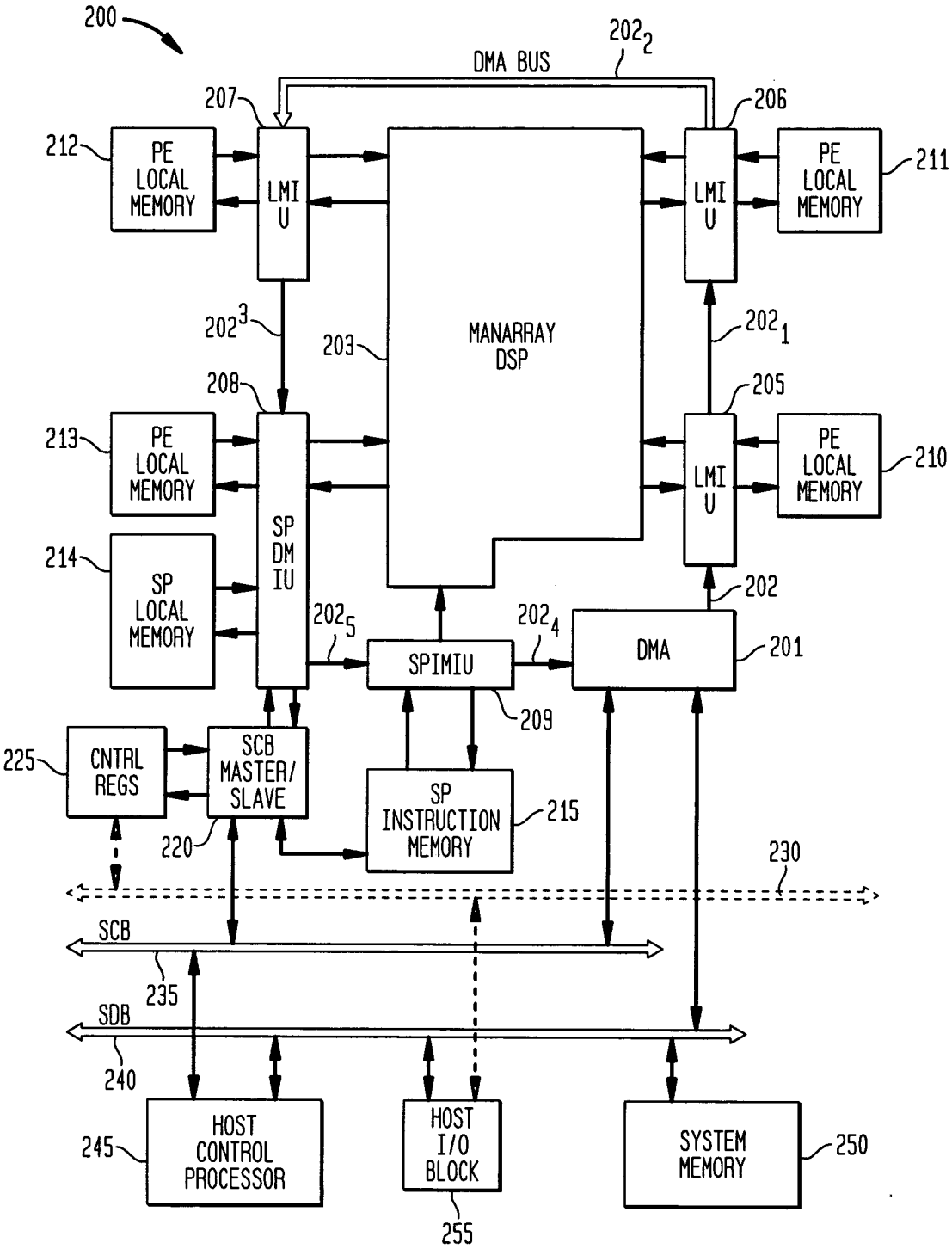

200
DMA BUS
202_2
207
206
212
PE LOCAL MEMORY
LMI U
MANARRAY DSP
LMI U
PE LOCAL MEMORY
211
202_3
203
202_1
208
205
213
PE LOCAL MEMORY
SP DM IU
LMI U
PE LOCAL MEMORY
210
214
SP LOCAL MEMORY
202
202_5
SPIMIU
202_4
DMA
201
209
225
CNTRL REGS
SCB MASTER/ SLAVE
SP INSTRUCTION MEMORY
215
220
230
SCB
235
SDB
240
245
HOST CONTROL PROCESSOR
HOST I/O BLOCK
255
SYSTEM MEMORY
250

FIG. 3

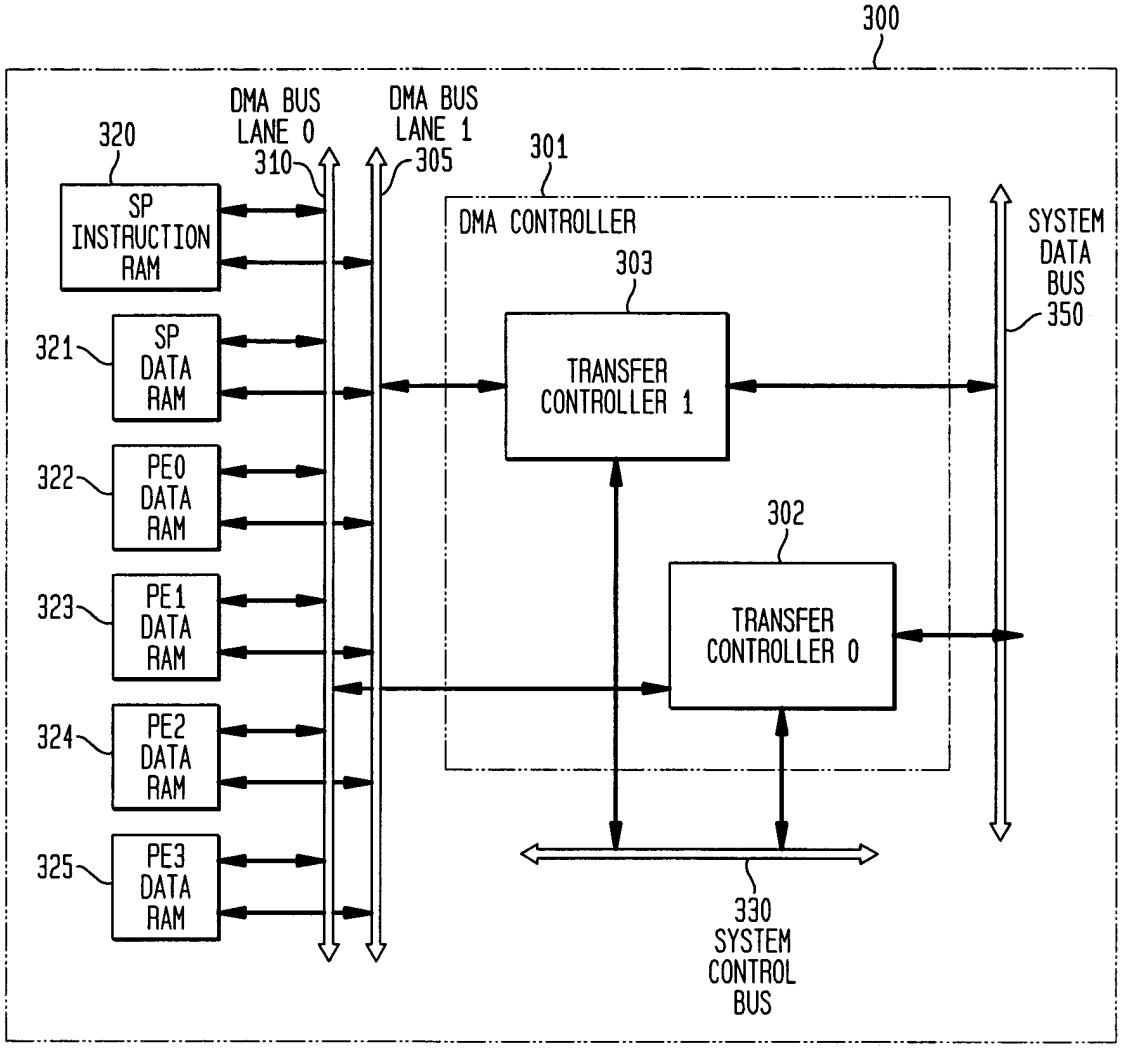

300
DMA BUS LANE 0
310
DMA BUS LANE 1
305
320
301
SP INSTRUCTION RAM
DMA CONTROLLER
303
SYSTEM DATA BUS
350
321
SP DATA RAM
TRANSFER CONTROLLER 1
322
PE0 DATA RAM
302
323
PE1 DATA RAM
TRANSFER CONTROLLER 0
324
PE2 DATA RAM
325
PE3 DATA RAM
330
SYSTEM CONTROL BUS

FIG. 4A

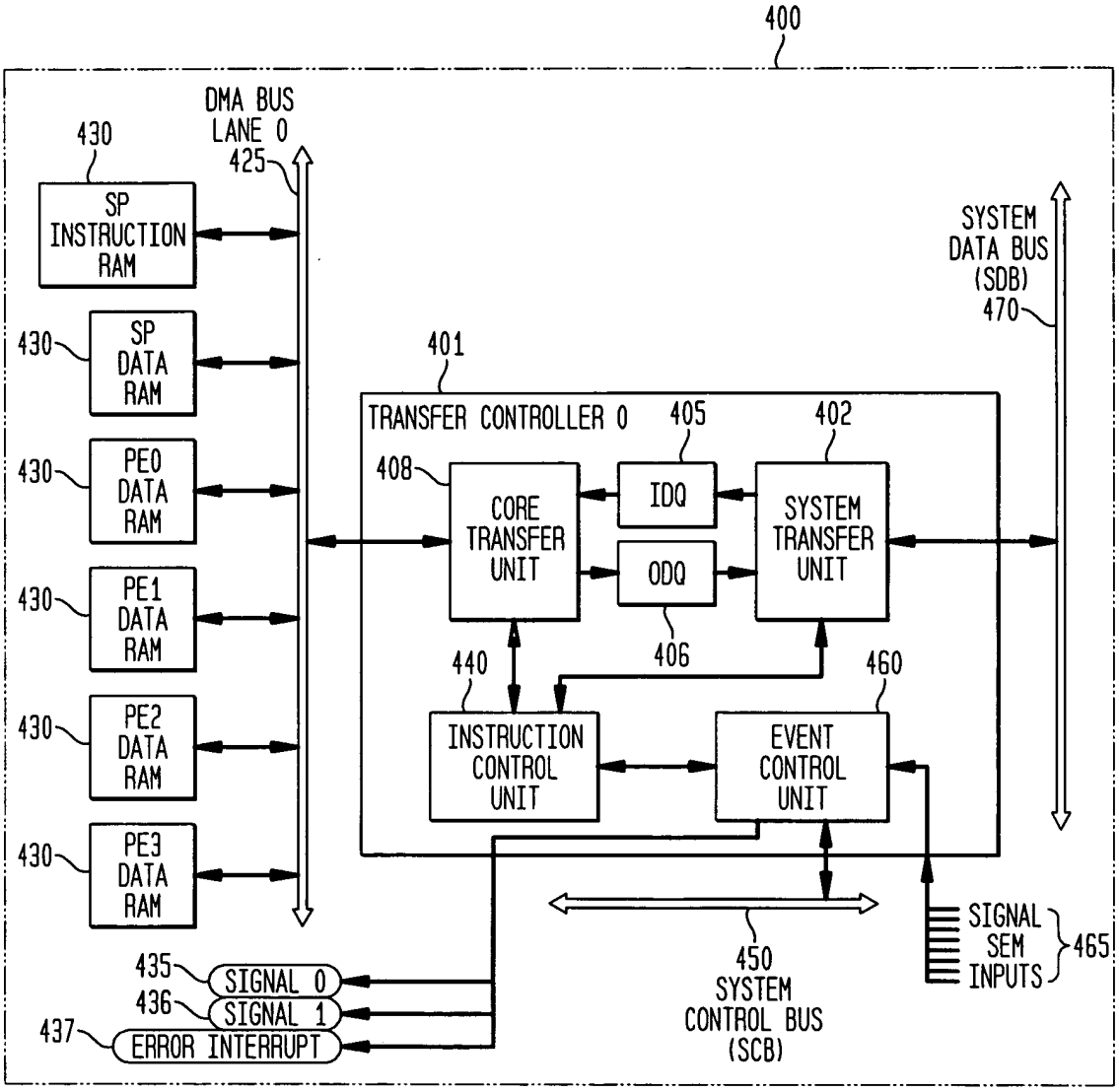

400
DMA BUS LANE 0
425
430
SP INSTRUCTION RAM
SP DATA RAM
PE0 DATA RAM
PE1 DATA RAM
PE2 DATA RAM
PE3 DATA RAM
SYSTEM DATA BUS (SDB)
470
401
TRANSFER CONTROLLER 0
405
402
408
CORE TRANSFER UNIT
IDQ
ODQ
406
SYSTEM TRANSFER UNIT
440
460
INSTRUCTION CONTROL UNIT
EVENT CONTROL UNIT
435
SIGNAL 0
436
SIGNAL 1
437
ERROR INTERRUPT
450
SYSTEM CONTROL BUS (SCB)
SIGNAL SEM INPUTS
465

FIG. 4B

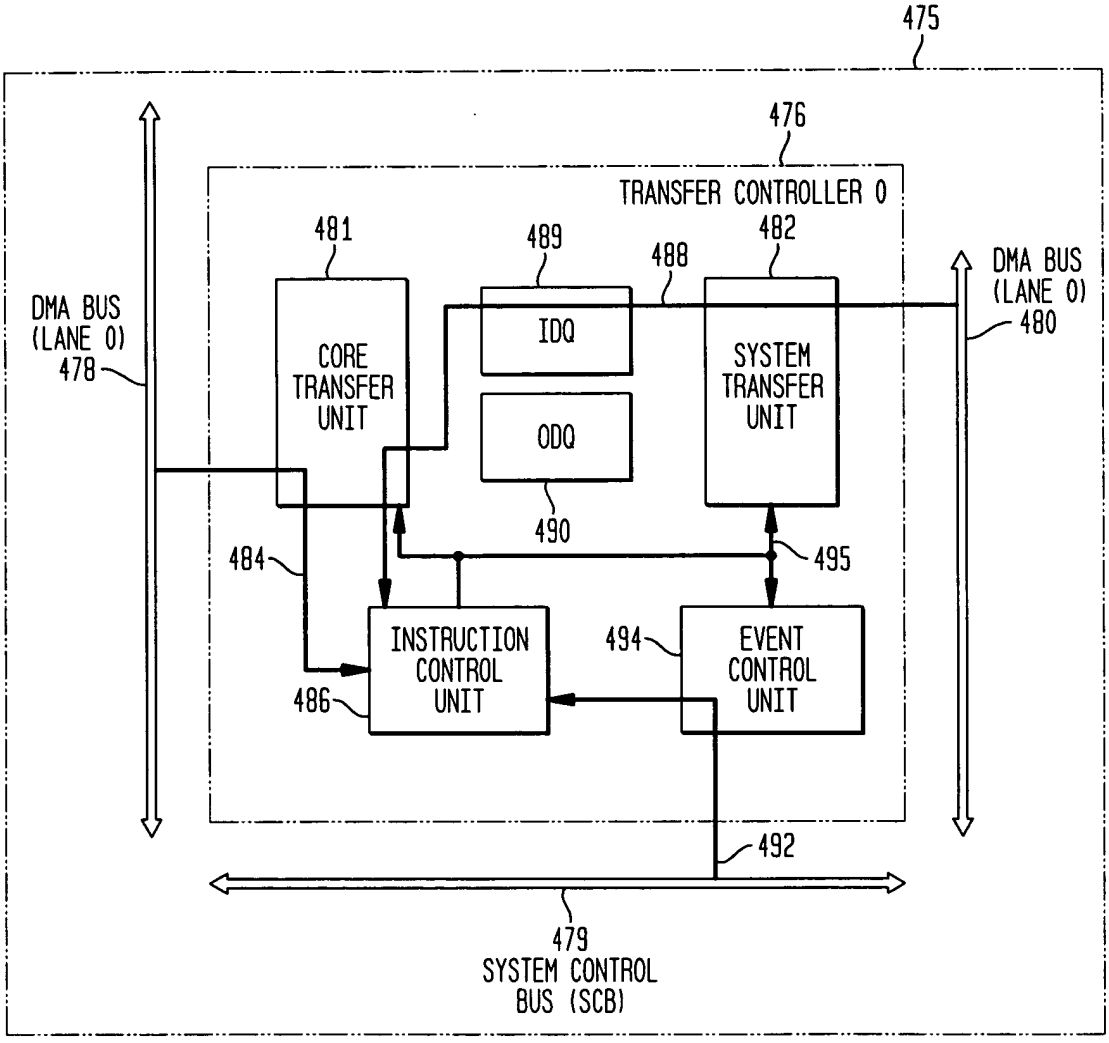

475
476
TRANSFER CONTROLLER 0
481
489
488
482
DMA BUS
(LANE 0)
478
CORE
TRANSFER
UNIT
IDQ
ODQ
490
SYSTEM
TRANSFER
UNIT
DMA BUS
(LANE 0)
480
484
495
INSTRUCTION
CONTROL
UNIT
486
494
EVENT
CONTROL
UNIT
492
479
SYSTEM CONTROL
BUS (SCB)

FIG. 4C

456 INSTRUCTION	457 OPERATION	458 DESCRIPTION
TRANSFER TYPE INSTRUCTIONS		
TSI	TRANSFER SYSTEM INBOUND	LOAD CONTROL PARAMETERS FOR INBOUND TRANSFER FROM SDB TO INBOUND FIFO.
TCI	TRANSFER CORE INBOUND	LOAD CONTROL PARAMETERS FOR INBOUND TRANSFER FROM INBOUND FIFO TO A CORE MEMORY.
TSO	TRANSFER SYSTEM OUTBOUND	LOAD CONTROL PARAMETERS FOR OUTBOUND TRANSFER FROM OUTBOUND FIFO TO SDB.
TCO	TRANSFER CORE OUTBOUND	LOAD CONTROL PARAMETERS FOR OUTBOUND TRANSFER FROM CORE MEMORY TO OUTBOUND FIFO.
439 BRANCH TYPE INSTRUCTIONS		
JMPcc	JUMP (PC-RELATIVE) CONDITIONAL	CONDITIONAL BRANCH TO A TPC-RELATIVE INSTRUCTION ADDRESS.
JMPDcc	JUMP (ABSOLUTE) CONDITIONAL	CONDITIONAL BRANCH TO AN ABSOLUTE TRANSFER INSTRUCTION ADDRESS (32 BIT).
CALLcc	CALL (PC-RELATIVE) CONDITIONAL	CONDITIONAL CALL. SAVE CURRENT TPC TO THE LINK PC (LINKPC) AND BRANCH TO A TPC-RELATIVE INSTRUCTION ADDRESS.
CALLDcc	CALL (ABSOLUTE) CONDITIONAL	CONDITIONAL CALL. SAVE CURRENT TPC TO THE LINK PC (LINKPC) AND BRANCH TO AN ABSOLUTE INSTRUCTION ADDRESS 32-BIT).
RETcc	RETURN CONDITIONAL	CONDITIONAL RETURN FROM CALL. RESTORE TPC FROM LINKPC AND FETCH THE NEXT INSTRUCTION FROM THE RESTORED ADDRESS.
STATE CONTROL TYPE INSTRUCTIONS		
RESTART	RESUME TRANSFER	RESTART SPECIFIED TRANSFER UNITS (CTU AND/OR STU).
CLEAR	CLEAR TRANSFER UNIT	SET STU, CTU OR BOTH TO AN INACTIVE STATE.
NOP	NO OPERATION	NO OPERATION (SKIP THIS INSTRUCTION)
SYNCHRONIZATION TYPE INSTRUCTIONS		
SIGNALcc	SIGNAL INTERRUPT, MESSAGE OR SEMAPHORE	SIGNAL WHEN A SEMAPHORE CONDITION IS TRUE. ALLOWS GENERAL CONDITIONAL SIGNALING USING INTERRUPTS, MESSAGE, OR SEMAPHORE UPDATES.
WAITcc	WAIT FOR SEMAPHORE CONDITION	WAIT WHILE A SEMAPHORE CONDITION IS TRUE. PROVIDES ATOMIC UPDATE.
LOAD TYPE INSTRUCTIONS		
PEXLAT	LOAD PE TRANSLATE TABLE	LOAD PE ID TRANSLATION TABLE. THIS TABLE IS USED DURING PE ADDRESSING MODES TO TRANSLATE PE ADDRESS BITS
BITREV	LOAD "BIT-REVERSED" INDEX TRANSLATE TABLE	LOAD CONFIGURATION BITS WHICH SPECIFY AN ADDRESS TRANSLATION SUPPORTING BIT REVERSAL OF INDICES FOR FFT COMPUTATIONS.
493 LIMEAR	LOAD EAR REGISTERS	LOADS EVENT-ACTION REGISTERS WITH IMMEDIATE VALUES. SETS UP CONDITIONS WHICH WILL TRIGGER SPECIFIED SIGNALING ACTIONS IN THE FORM OF INTERRUPTS, MESSAGES AND/OR SEMAPHORE UPDATES.
LIMGR	LOAD IMMEDIATE GENERAL REGISTER	LOADS ONE OR MORE GENERAL REGISTERS (GR0-GR3) WITH IMMEDIATE VALUES.
LIMSEM	LOAD SEMAPHORE REGISTERS	THIS INSTRUCTION ALLOWS LOADING OF SEMAPHORE REGISTERS WITH IMMEDIATE VALUES.

FIG. 4D

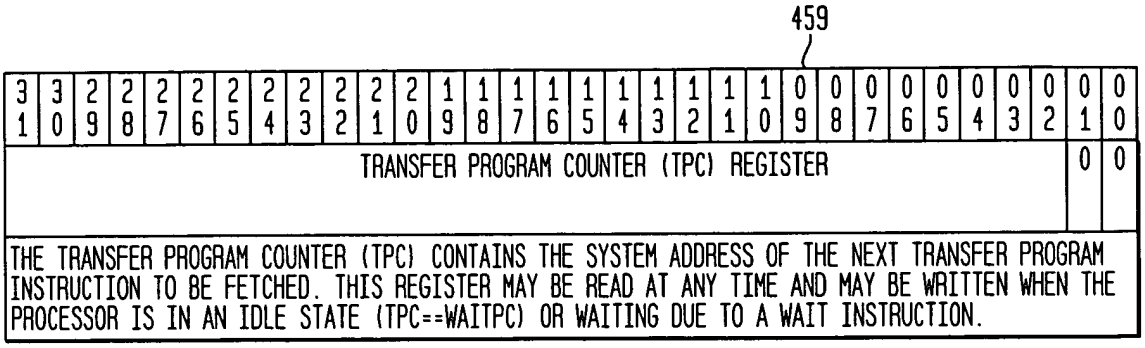

459
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
TRANSFER PROGRAM COUNTER (TPC) REGISTER
0 0
THE TRANSFER PROGRAM COUNTER (TPC) CONTAINS THE SYSTEM ADDRESS OF THE NEXT TRANSFER PROGRAM INSTRUCTION TO BE FETCHED. THIS REGISTER MAY BE READ AT ANY TIME AND MAY BE WRITTEN WHEN THE PROCESSOR IS IN AN IDLE STATE (TPC==WAITPC) OR WAITING DUE TO A WAIT INSTRUCTION.

FIG. 4E

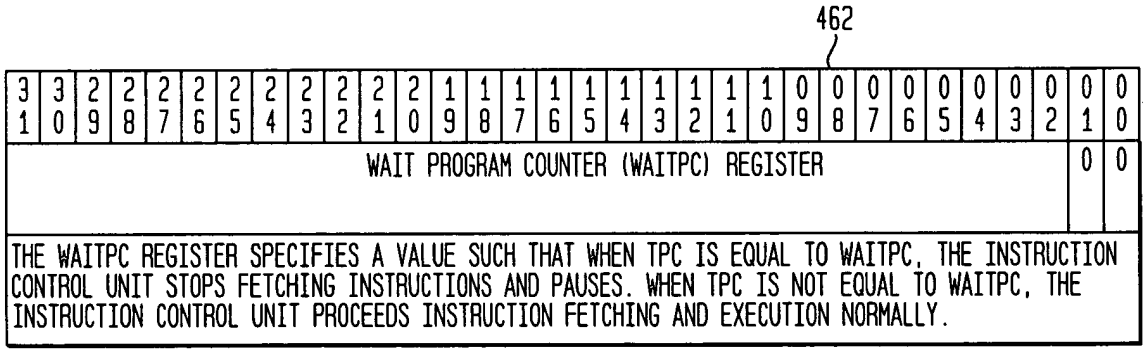

462
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
WAIT PROGRAM COUNTER (WAITPC) REGISTER
0 0
THE WAITPC REGISTER SPECIFIES A VALUE SUCH THAT WHEN TPC IS EQUAL TO WAITPC, THE INSTRUCTION CONTROL UNIT STOPS FETCHING INSTRUCTIONS AND PAUSES. WHEN TPC IS NOT EQUAL TO WAITPC, THE INSTRUCTION CONTROL UNIT PROCEEDS INSTRUCTION FETCHING AND EXECUTION NORMALLY.

FIG. 4F1

496

NAME	SYSTEM ADDRESS	DESCRIPTION
	TRANSFER CONTROLLER	
BASE ADDRESS (EXAMPLE)	0x00708000	
	REGISTER OFFSET	
RESUME	0x03	WRITE-ONLY ADDRESS. CAUSES THE TRANSFER CONTROLLER TO RESUME FETCHING AND DECODING INSTRUCTIONS WHEN IT IS IN THE WAIT STATE DUE TO A WAIT INSTRUCTION. THIS COMMAND OVERRIDES ANY CONDITION SPECIFIED IN THE WAIT INSTRUCTION.
497 CLEAR	0x04	WRITE-ONLY ADDRESS. CLEARS BOTH STU AND CTU OF TRANSFER PARAMETERS AND PLACES THEM IN THE INACTIVE STATE.
CLEARSTU	0x05	WRITE-ONLY ADDRESS. CLEARS STU OF TRANSFER PARAMETERS AND PLACES IT INTO THE INACTIVE STATE
CLEARCTU	0x06	WRITE-ONLY ADDRESS. CLEARS CTU OF TRANSFER PARAMETERS AND PLACES IT INTO THE INACTIVE STATE.
498 RESTART	0x07	WRITE-ONLY ADDRESS. CAUSE BOTH STU AND CTU TO PERFORM A RESTART. IF EITHER TRANSFER UNIT HAS A ZERO CURRENT TRANSFER COUNT, THEN IT CURRENT COUNT IS RELOADED FROM ITS INITIAL TRANSFER COUNT. THE CURRENT TRANSFER PARAMETERS ARE USED TO RESTART AND CONTINUE THE TRANSFER, AND ALL OTHER PARAMETERS REMAIN THE SAME.
501 RESTARTSTU	0x08	WRITE-ONLY ADDRESS. CAUSE STU TO PERFORM A RESTART. IF THE STC IS ZERO, RELOAD FROM ISTC. IF CTC HAS NON-ZERO TRANSFER COUNT, THEN CONTINUE TRANSFER. IF CTC HAS ZERO TRANSFER COUNT, REMAIN IN CURRENT TRANSFER STATE.
RESTARTCTU	0x09	WRITE-ONLY ADDRESS. CAUSE CTU TO PERFORM A RESTART. IF THE CTC IS ZERO, RELOAD FROM ICTC. IF STC HAS NON-ZERO TRANSFER COUNT, THEN CONTINUE TRANSFER. IF STC HAS ZERO TRANSFER COUNT, REMAIN IN CURRENT TRANSFER STATE.
RESET	0x20	WRITE-ONLY ADDRESS. CAUSES RESET OF TRANSFER CONTROLLER. ALL REGISTERS INTIALIZED. TPC SET EQUAL TO WAITPC.
INITSTC	0x30	WRITE-ONLY ADDRESS + DATA (UPDATES BOTH STC AND ISTC).
499 INITSTC_START	0x31	WRITE-ONLY ADDRESS + DATA (UPDATES BOTH STC AND ISTC, THEN RESTARTS TRANSFER)
INITCTC	0x34	WRITE-ONLY ADDRESS + DATA (UPDATES BOTH CTC AND ICTC).
INITCTC_START	0x35	WRITE-ONLY ADDRESS + DATA (UPDATES BOTH CTC AND ICTC, THEN RESTARTS TRANSFER)
WRITESTC	0x38	WRITE-ONLY ADDRESS + DATA (UPDATES BOTH STC, NOT ISTC).
WRITESTC_START	0x39	WRITE-ONLY ADDRESS + DATA (UPDATES BOTH STC, NOT

FIG. 4F2

	WRITECTC	0x3c	WRITE-ONLY ADDRESS + DATA (UPDATES ONLY CTC NOT ICTC).
	WRITECTC_START	0x3d	WRITE-ONLY ADDRESS + DATA (UPDATES ONLY CTC NOT ICTC, THEN RESTARTS TRANSFER)
464	LOCKID0	0x50	READ-ADDRESS. READ RETURNS 1 IF LOCKED, 0 IF NOT LOCKED (LOCK GRANTED)
464	LOCKID1	0x51	READ-ADDRESS. READ RETURNS 1 IF LOCKED, 0 IF NOT LOCKED (LOCK GRANTED)
464	LOCKID2	0x52	READ-ADDRESS. READ RETURNS 1 IF LOCKED, 0 IF NOT LOCKED (LOCK GRANTED)
464	LOCKID3	0x53	READ-ADDRESS. READ RETURNS 1 IF LOCKED, 0 IF NOT LOCKED (LOCK GRANTED)
464	LOCKID4	0x54	READ-ADDRESS. READ RETURNS 1 IF LOCKED, 0 IF NOT LOCKED (LOCK GRANTED)
464	LOCKID5	0x55	READ-ADDRESS. READ RETURNS 1 IF LOCKED, 0 IF NOT LOCKED (LOCK GRANTED)
464	LOCKID6	0x56	READ-ADDRESS. READ RETURNS 1 IF LOCKED, 0 IF NOT LOCKED (LOCK GRANTED)
464	LOCKID7	0x57	READ-ADDRESS. READ RETURNS ZERO IF LOCKED, 8 IF NOT LOCKED (LOCK GRANTED)
	UWAITS0	0x60	READ-ADDRESS. IF SPECIFIED SEMAPHORE IS ZERO, RETURNS 0 FOR THE READ. IF SPECIFIED SEMAPHORE IS NON-ZERO, RETURN VALUE AND DECREMENT SEMAPHORE.
491	INCS0	0x60	WRITE ADDRESS. INCREMENT SPECIFIED SEMAPHORE.
	UWAITS1	0x61	READ-ADDRESS. IF SPECIFIED SEMAPHORE IS ZERO, RETURNS 0 FOR THE READ. IF SPECIFIED SEMAPHORE IS NON-ZERO, RETURN VALUE AND DECREMENT SEMAPHORE.
	INCS1	0x61	WRITE ADDRESS. INCREMENT SPECIFIED SEMAPHORE.
	UWAITS2	0x62	READ-ADDRESS. IF SPECIFIED SEMAPHORE IS ZERO, RETURNS 0 FOR THE READ. IF SPECIFIED SEMAPHORE IS NON-ZERO, RETURN VALUE AND DECREMENT SEMAPHORE.
	INCS2	0x62	WRITE ADDRESS. INCREMENT SPECIFIED SEMAPHORE.
	UWAITS3	0x63	READ-ADDRESS. IF SPECIFIED SEMAPHORE IS ZERO, RETURNS 0 FOR THE READ. IF SPECIFIED SEMAPHORE IS NON-ZERO, RETURN VALUE AND DECREMENT SEMAPHORE.
	INCS3	0x63	WRITE ADDRESS. INCREMENT SPECIFIED SEMAPHORE.
	SWAITS0	0x64	READ-ADDRESS. SEMAPHORE IS TREATED AS A SIGNED TWO-COMPLEMENT INTEGER. IF SPECIFIED SEMAPHORE IS GREATER THAN ZERO, RETURN ITS VALUE THEN DECREMENT BY 1. IF LESS THAN OR EQUAL TO ZERO, RETURN VALUE AND DO NOT DECREMENT.
	DECS0	0x64	WRITE ADDRESS. DECREMENT SPECIFIED SEMAPHORE.
	SWAITS1	0x65	READ-ADDRESS. SEMAPHORE IS TREATED AS A SIGNED TWO-COMPLEMENT INTEGER. IF SPECIFIED SEMAPHORE IS GREATER THAN ZERO, RETURN ITS VALUE THEN DECREMENT BY 1. IF LESS THAN OR EQUAL TO ZERO, RETURN VALUE AND DO NOT DECREMENT.
	DECS1	0x65	WRITE ADDRESS. DECREMENT SPECIFIED SEMAPHORE.

FIG. 4F3

SWAITS2	0x66	READ-ADDRESS. SEMAPHORE IS TREATED AS A SIGNED TWO-COMPLEMENT INTEGER. IF SPECIFIED SEMAPHORE IS GREATER THAN ZERO, RETURN ITS VALUE THEN DECREMENT BY 1. IF LESS THAN OR EQUAL TO ZERO, RETURN VALUE AND DO NOT DECREMENT.
DECS2	0x66	WRITE ADDRESS. DECREMENT SPECIFIED SEMAPHORE.
SWAITS3	0x67	READ-ADDRESS. SEMAPHORE IS TREATED AS A SIGNED TWO-COMPLEMENT INTEGER. IF SPECIFIED SEMAPHORE IS GREATER THAN ZERO, RETURN ITS VALUE THEN DECREMENT BY 1. IF LESS THAN OR EQUAL TO ZERO, RETURN VALUE AND DO NOT DECREMENT.
DECS3	0x67	WRITE ADDRESS. DECREMENT SPECIFIED SEMAPHORE.
CLEARS0	0x68	READ ADDRESS. READ CAUSES CLEAR OF SPECIFIED SEMAPHORE. RETURNS VALUE PRIOR TO CLEARING.
SETS0	0x68	WRITE ADDRESS. WRITE CAUSES SET OF SPECIFIED SEMAPHORE TO A VALUE OF 1.
CLEARS1	0x69	READ ADDRESS. READ CAUSES CLEAR OF SPECIFIED SEMAPHORE. RETURNS VALUE PRIOR TO CLEARING.
SETS1	0x69	WRITE ADDRESS. WRITE CAUSES SET OF SPECIFIED SEMAPHORE TO A VALUE OF 1.
CLEARS2	0x6a	READ ADDRESS. READ CAUSES CLEAR OF SPECIFIED SEMAPHORE. RETURNS VALUE PRIOR TO CLEARING.
SETS2	0x6a	WRITE ADDRESS. WRITE CAUSES SET OF SPECIFIED SEMAPHORE TO A VALUE OF 1.
CLEARS3	0x6b	READ ADDRESS. READ CAUSES CLEAR OF SPECIFIED SEMAPHORE. RETURNS VALUE PRIOR TO CLEARING.
SETS3	0x6b	WRITE ADDRESS. WRITE CAUSES SET OF SPECIFIED SEMAPHORE TO A VALUE OF 1.
INITPC (463)	0x100	WRITE-ONLY ADDRESS + DATA. VALUE IS WRITTEN TO BOTH TPC AND WAITPC AND IS INTERPRETED AS A DMA INSTRUCTION ADDRESS.
WAITPC	0x104	READ/WRITE WAITPC REGISTER.
TPC	0x108	READ/WRITE TPC REGISTER.
LINKPC	0x10c	READ/WRITE ADDRESS FOR LINKPC REGISTER.
SEM	0x110	READ/WRITE SEM (S0,S1,S2,S3) REGISTER.
EAR0	0x114	READ/WRITE ADDRESS FOR EAR0 REGISTER.
EAR1	0x118	READ/WRITE ADDRESS FOR EAR1 REGISTER.
BITREV	0x11c	READ/WRITE ADDRESS FOR "BIT-REVERSE" ADDRESS MODE REGISTER.
GR0	0x120	READ/WRITE GENERAL REGISTER 0
GR1	0x124	READ/WRITE GENERAL REGISTER 1
GR2	0x128	READ/WRITE GENERAL REGISTER 2
GR3	0x12c	READ/WRITE GENERAL REGISTER 3
PETABLE	0x130	READ/WRITE ADDRESS PE ID TRANSLATION TABLE
ITCNT	0x134	READ/WRITE ADDRESS FOR INITIAL TRANSFER COUNT REGISTER (CONTAINS BOTH ISTC AND ICTC).

FIG. 4F4

TCNT	0x138	READ/WRITE ADDRESS FOR CURRENT TRANSFER COUNT REGISTER (CONTAINS BOTH STC AND CTC).
LOCK	0x13c	READ-ONLY ADDRESS FOR RETURNING CURRENT OWNER OF THE WAITPC LOCK.
TSR	0x140	READ-ONLY. TRANSFER CONTROLLER STATUS REGISTER.
EXTSIG	0x150	READ/WRITE EXTERNAL SIGNAL SELECT AND ENABLE REGISTER.

FIG. 5A

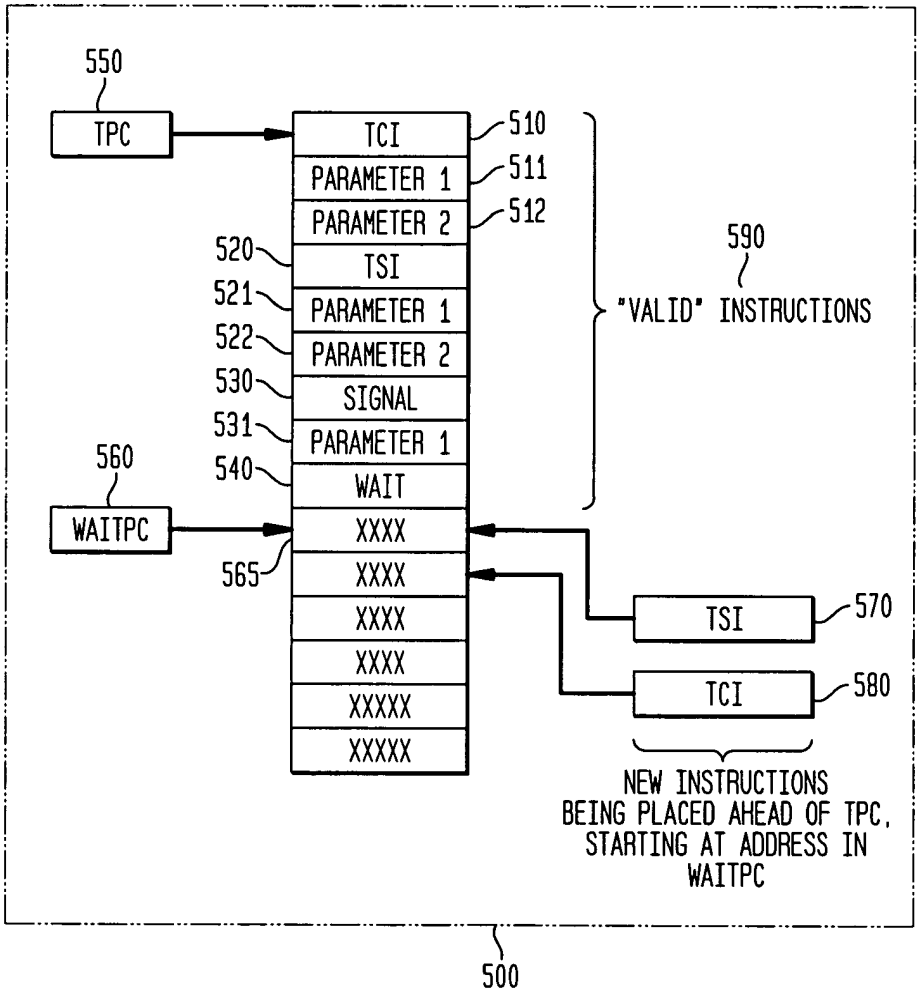
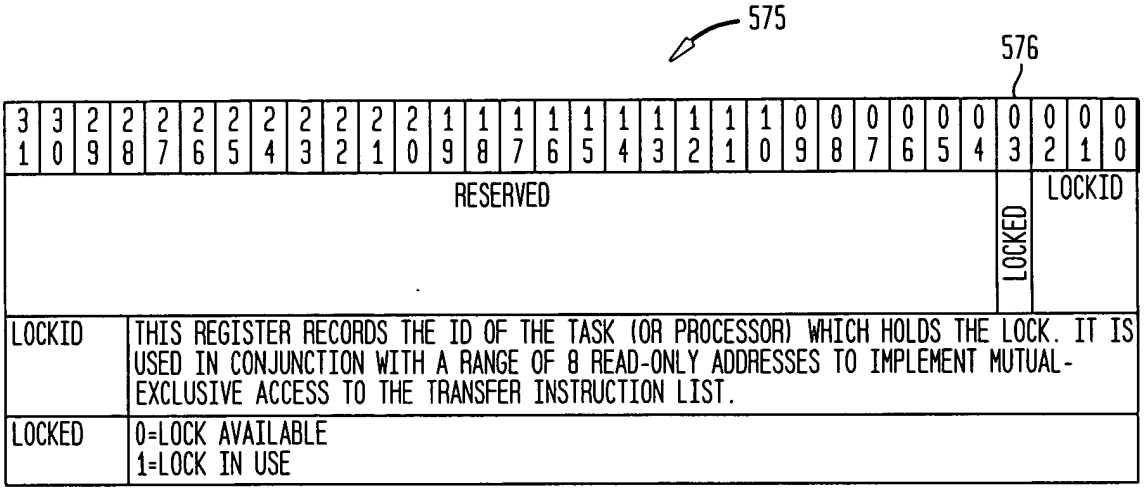
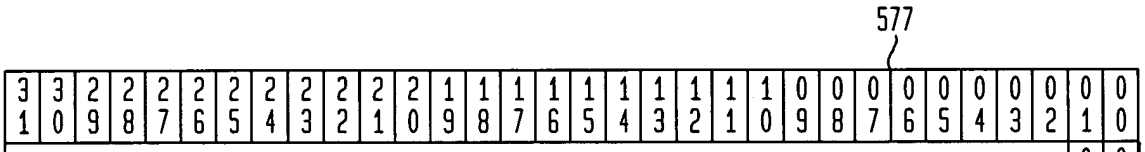


FIG. 5B



LOCKID	THIS REGISTER RECORDS THE ID OF THE TASK (OR PROCESSOR) WHICH HOLDS THE LOCK. IT IS USED IN CONJUNCTION WITH A RANGE OF 8 READ-ONLY ADDRESSES TO IMPLEMENT MUTUAL-EXCLUSIVE ACCESS TO THE TRANSFER INSTRUCTION LIST.
LOCKED	0=LOCK AVAILABLE 1=LOCK IN USE

FIG. 5C



THE LINKPC REGISTER IS USED TO SAVE THE ADDRESS OF THE NEXT INSTRUCTION TO BE EXECUTED AFTER A CALL INSTRUCTION. EXECUTING THE CALL INSTRUCTION (WHEN THE CALL CONDITION IS TRUE) CAUSES THE ADDRESS OF THE NEXT INSTRUCTION AFTER TO CALL (WHOSE ADDRESS IS CALLED THE "RETURN ADDRESS") TO BE COPIED TO THE LINKPC. WHEN THE SUBROUTINE IS COMPLETE, A RET (RETURN) INSTRUCTION IS EXECUTED WHICH RESTORES THE SAVED TPC VALUE FROM THE LINKPC REGISTER CAUSING A DIRECT BRANCH BACK TO THE RETURN ADDRESS.

FIG. 5D

578

SEMAPHORE CONDITION	ALWAYS EQUAL NOT EQUAL HIGHER THAN HIGHER THAN OR EQUAL LOWER THAN LOWER THAN OR EQUAL CTUeot (CTU AT END-OF-TRANSFER) STUeot (STU AT END-OF-TRANSFER) NotCTUeot (CTU NOT AT END-OF-TRANSFER) NotSTUeot (STU NOT AT END-OF-TRANSFER) GREATER THAN OR EQUAL GREATER THAN LESS THAN OR EQUAL LESS THAN

FIG. 5E

579

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
S3								S2								S1								S0							

THE SEMAPHORE REGISTERS ARE USED TO GENERATE CONDITIONS FOR ALL CONDITIONAL INSTRUCTIONS, AND PROCESSOR-TRANSFER SYNCHRONIZATION. THESE REGISTERS MAY BE READ/WRITTEN (AS A GROUP) DIRECTLY AT THE SEM ADDRESS, OR INDIRECTLY AT OTHER READ/WRITE ADDRESSES WHICH CAUSE SPECIFIC SEMAPHORE SIDE-EFFECTS. THE LIMSEM INSTRUCTION ALSO MAY BE USED TO LOAD AN IMMEDIATE VALUE INTO ANY OR ALL OF THESE REGISTERS, DIFFFERENT IMPLEMENTATIONS MAY HAVE A GREATER OR LESSER NUMBER OF SEMAPHORE REGISTERS AND THERE IS NO SPECIAL RESTRICTION ON SIZE. A PREFERRED EMBODIMENT USES FOUR 8-BIT SEMAPHORE REGISTERS.

S0	SEMAPHORE REGISTER 0
S1	SEMAPHORE REGISTER 1
S2	SEMAPHORE REGISTER 2
S3	SEMAPHORE REGISTER 3

FIG. 6

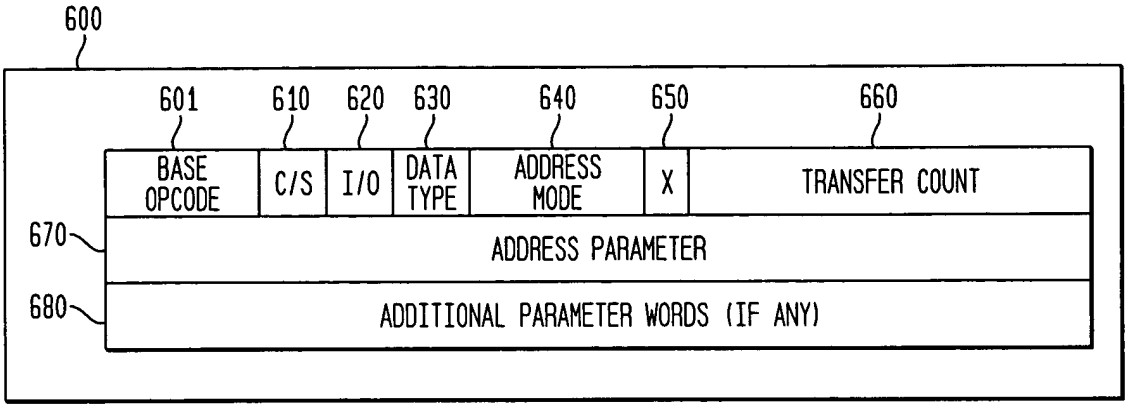

600
601
610
620
630
640
650
660
BASE OPCODE
C/S
I/O
DATA TYPE
ADDRESS MODE
X
TRANSFER COUNT
670
ADDRESS PARAMETER
680
ADDITIONAL PARAMETER WORDS (IF ANY)

FIG. 7

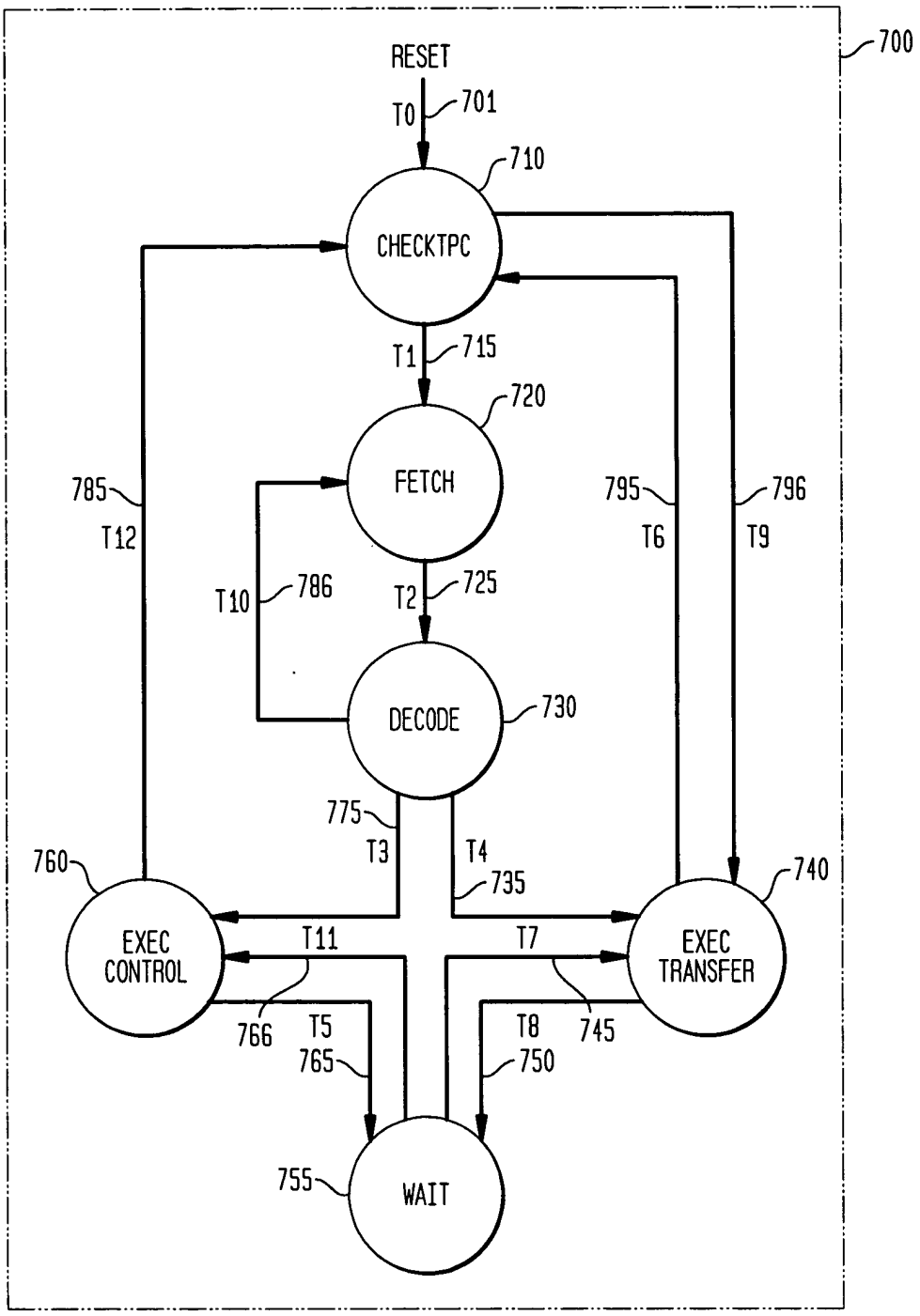

700
RESET
T0
701
710
CHECKTPC
T1
715
720
FETCH
785
T12
795
T6
796
T9
T10
786
T2
725
DECODE
730
775
T3
T4
735
760
740
EXEC CONTROL
T11
T7
EXEC TRANSFER
766
T5
765
T8
745
750
755
WAIT

FIG. 8A

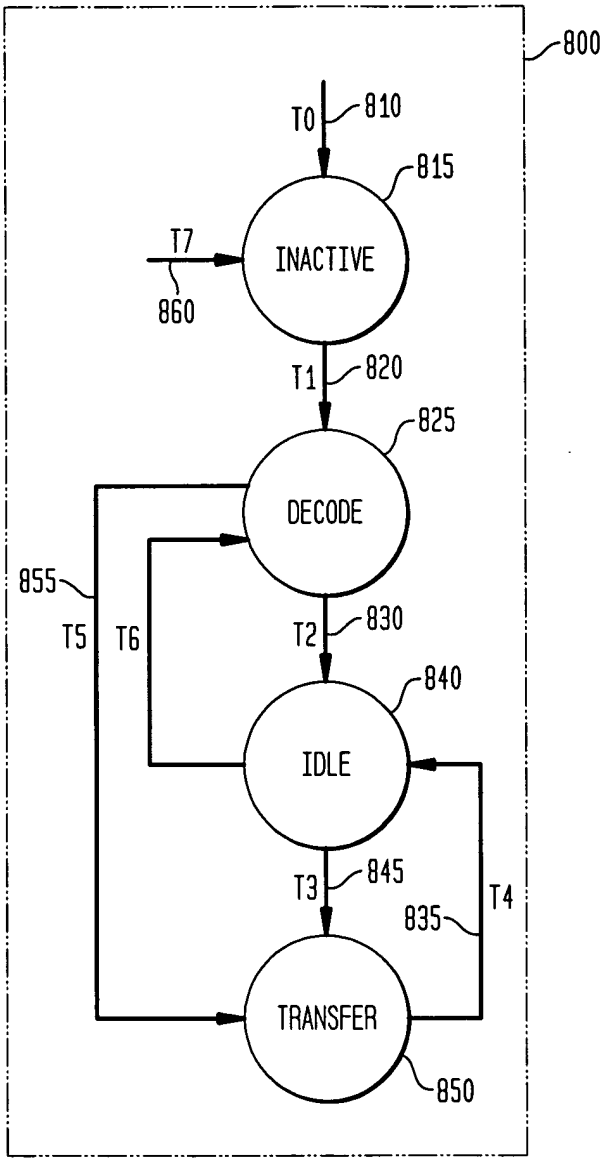

800
T0
810
815
INACTIVE
T7
860
T1
820
825
DECODE
855
T5
T6
T2
830
840
IDLE
T3
845
T4
835
TRANSFER
850

FIG. 8B

875

tsi.block tc=200, addr=0x00010000;	TRANSFER-SYSTEM-INBOUND. STU RECEIVES THIS INSTRUCTION AND LOADS PARAMETERS. TRANSFER FROM SYSTEM DATA BUS TO INBOUND DATA QUEUE (IDQ). TRANSFER COUNT IS 200 UNITS, SYSTEM DATA BUS ADDRESS IS 0x00010000;
tci.block.x tc=200, addr=0x0010;	TRANSFER-CORE-INBOUND INSTRUCTION. CTU RECEIVES THIS INSTRUCTION AND LOADS PARAMETERS. TRANSFER FROM INPUT DATA QUEUE TO THE DMA BUS USING BLOCK ADDRESS MODE (SEQUENTIAL ADDRESSES). TRANSFER COUNT IS 100 UNITS AND STARTING DMA BUS ADDRESS IS 0x0010. THE '.X' EXTENSION CAUSES THE "EXECUTE" BIT TO BE SET SO THAT BOTH THE STU AND CTU ARE STARTED IMMEDIATELY AFTER LOADING THIS INSTRUCTION.

FIG. 8C

885

tsi.block tc=200, addr=0x00010000;	TRANSFER-SYSTEM-INBOUND. STU RECEIVES THIS INSTRUCTION AND LOADS PARAMETERS. TRANSFER FROM SYSTEM DATA BUS TO INBOUND DATA QUEUE (IDQ). TRANSFER COUNT IS 200 UNITS, SYSTEM DATA BUS ADDRESS IS 0x00010000;
tci.block tc=200, addr=0x0010;	TRANSFER-CORE-INBOUND INSTRUCTION. CTU RECEIVES THIS INSTRUCTION AND LOADS PARAMETERS. TRANSFER FROM INPUT DATA QUEUE TO THE DMA BUS USING BLOCK ADDRESS MODE (SEQUENTIAL ADDRESSES). TRANSFER COUNT IS 100 UNITS AND STARTING DMA BUS ADDRESS IS 0x0010. SINCE THERE IS NO "x" EXTENSION, THE TRANSFER DOES NOT BEGIN IMMEDIATELY.
WAIT;	WAIT UNTIL HOST PROCESSOR PERFORMS A RESTART ACTION.

FIG. 9A

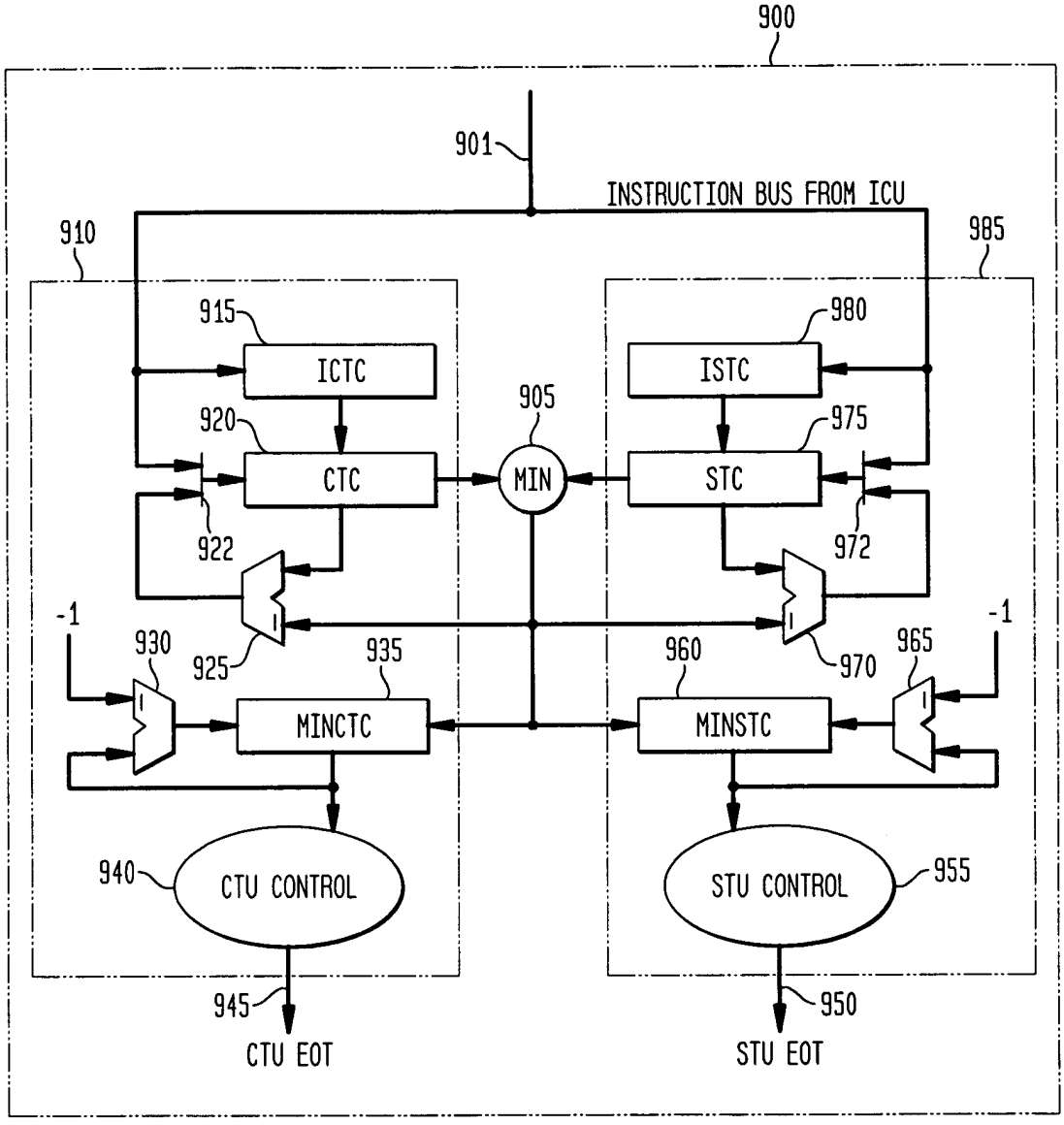

900
901
INSTRUCTION BUS FROM ICU
910
985
915
ICTC
980
ISTC
905
920
CTC
MIN
975
STC
922
972
-1
930
925
935
960
970
965
-1
MINCTC
MINSTC
940
CTU CONTROL
STU CONTROL
955
945
950
CTU EOT
STU EOT

FIG. 9B

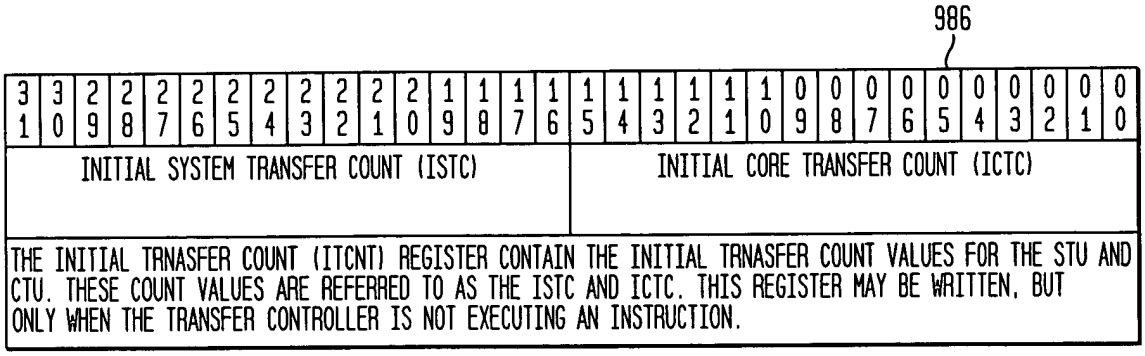

986
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
INITIAL SYSTEM TRANSFER COUNT (ISTC)
INITIAL CORE TRANSFER COUNT (ICTC)
THE INITIAL TRNASFER COUNT (ITCNT) REGISTER CONTAIN THE INITIAL TRNASFER COUNT VALUES FOR THE STU AND CTU. THESE COUNT VALUES ARE REFERRED TO AS THE ISTC AND ICTC. THIS REGISTER MAY BE WRITTEN, BUT ONLY WHEN THE TRANSFER CONTROLLER IS NOT EXECUTING AN INSTRUCTION.

FIG. 9C

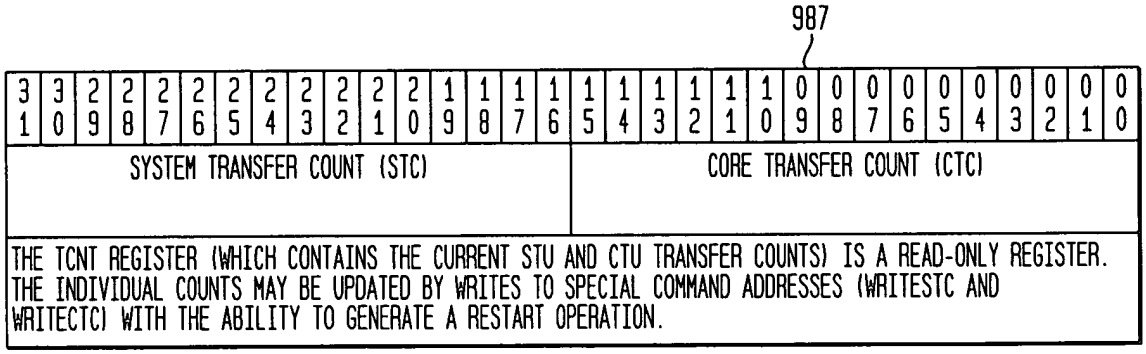

987
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
SYSTEM TRANSFER COUNT (STC)
CORE TRANSFER COUNT (CTC)
THE TCNT REGISTER (WHICH CONTAINS THE CURRENT STU AND CTU TRANSFER COUNTS) IS A READ-ONLY REGISTER. THE INDIVIDUAL COUNTS MAY BE UPDATED BY WRITES TO SPECIAL COMMAND ADDRESSES (WRITESTC AND WRITECTC) WITH THE ABILITY TO GENERATE A RESTART OPERATION.

FIG. 9D

988

tso.block tc =200, addr=0x00010000;	TRANSFER-SYSTEM-INBOUND. STU RECEIVES THIS INSTRUCTION AND LOADS PARAMETERS. TRANSFER FROM ODQ TO SYSTEM DATA BUS. TRANSFER COUNT IS 200 UNITS, SYSTEM DATA BUS ADDRESS IS 0x00010000;
tso.block.x tc =50, addr=0x00000310;	TRANSFER-CORE-OUTBOUND INSTRUCTION. TRANSFER 50 DATA ELEMENTS, FROM SPECIFIED LOCAL MEMORY ADDRESS IN BLOCK ADDRESSING MODE. START TRANSFER IMMEDIATELY.
tso.block.x tc=50, addr=0x00200400;	TRANSFER-CORE-OUTBOUND INSTRUCTION. TRANSFER 50 DATA ELEMENTS, FROM SPECIFIED LOCAL MEMORY ADDRESS IN BLOCK ADDRESSING MODE. START TRANSFER IMMEDIATELY.
tso.stride.x tc=50, addr=0x00210200, sride=16, hold=10;	TRANSFER-CORE-OUTBOUND INSTRUCTION. TRANSFER 50 DATA ELEMENTS, FROM SPECIFIED LOCAL MEMORY ADDRESS IN STRIDE ADDRESSING MODE. START TRANSFER IMMEDIATELY.
tso.circ.x tc=50, addr=0x00230600, bufinit=0, bufsize=128;	TRANSFER-CORE-OUTBOUND INSTRUCTION. TRANSFER 50 DATA ELEMENTS, FROM SPECIFIED LOCAL MEMORY ADDRESS IN CIRCULAR ADDRESSING MODE. START TRANSFER IMMEDIATELY.
wait;	WAIT HERE AFTER TRANSFERS.

FIG. 9E

989

tso.block tc =200, addr=0x00010000;	TRANSFER-CORE-OUTBOUND. CTU RECEIVES THIS INSTRUCTION AND LOADS PARAMETERS. TRANSFER FROM DMA BUS TO ODQ. TRANSFER COUNT IS 200 UNITS, DMA BUS ADDRESS IS 0x00010000;
tso.block.x tc =50, addr=0x00000310;	TRANSFER-SYSTEM-OUTBOUND INSTRUCTION. TRANSFER 50 DATA ELEMENTS, FROM ODQ TO SPECIFIED SDB ADDRESS IN BLOCK ADDRESSING MODE. START TRANSFER IMMEDIATELY.
tso.block.x tc=50, addr=0x00200400;	TRANSFER-SYSTEM-OUTBOUND INSTRUCTION. TRANSFER 50 DATA ELEMENTS, FROM ODQ TO SPECIFIED SDB ADDRESS IN BLOCK ADDRESSING MODE. START TRANSFER IMMEDIATELY.
tso.stride.x tc=50, addr=0x00210200, sride=16, hold=10;	TRANSFER-SYSTEM-OUTBOUND INSTRUCTION. TRANSFER 50 DATA ELEMENTS, FROM ODQ TO SPECIFIED SDB ADDRESS IN STRIDE ADDRESSING MODE. START TRANSFER IMMEDIATELY.
tso.circ.x tc=50, addr=0x00230600, bufinit=0, bufsize=128;	TRANSFER-SYSTEM-OUTBOUND INSTRUCTION. TRANSFER 50 DATA ELEMENTS, FROM ODQ TO SPECIFIED SDB ADDRESS IN CIRCULAR ADDRESSING MODE. START TRANSFER IMMEDIATELY.
wait;	WAIT HERE AFTER TRANSFERS.

FIG. 9F

990

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RESERVED																S3 SigEn	S3 ExtSig Select			S2 SigEn	S2 ExtSig Select			S1 SigEn	S1 ExtSig Select			S0 SigEn	S0 ExtSig Select		

THE EXTERNAL SIGNAL REGISTER ALLOWS THE SELECTION OF 1 OUT OF N EXTERNAL INPUT SIGNALS WHICH, WHEN ASSERTED FOR ONE CLOCK-CYCLE, WILL CAUSE THE CORRESPONDING SEMAPHORE TO BE INCREMENTED BY 1. THE ABOVE REGISTER ALLOWS FOR UP TO 8 EXTERNAL SIGNALS, ONE OF WHICH CAN BE ROUTED AS A SIGNAL INPUT TO EACH SEMAPHORE REGISTER.

S0 ExtSig Select	S0 EXTERNAL SIGNAL SELECT. SPECIFIES WHICH OF 8 EXTERNAL INPUT SIGNALS WILL GENERATE A SIGNAL TO UPDATE SEMAPHORE REGISTER. (SEE TABLE BELOW)
S0 SigEn	S0 EXTERNAL SIGNAL ENABLE. 0 = DISABLED. EXTERNAL SIGNAL HAS NO EFFECT ON SEMAPHORE. 1 = ENABLED. WHEN EXTERNAL SIGNAL SPECIFIED BY S0 ExtSig Select IS ASSERTED HIGH FOR 1 CLOCK PERIOD, SEMAPHORE REGISTER S0 IN INCREMENTED.
S1 ExtSig Select	S1 EXTERNAL SIGNAL SELECT. SPECIFIES WHICH OF 8 EXTERNAL INPUT SIGNALS WILL GENERATE A SIGNAL TO UPDATE SEMAPHORE REGISTER. (SEE TABLE BELOW)
S1 SigEn	S1 EXTERNAL SIGNAL ENABLE. 0 = DISABLED. EXTERNAL SIGNAL HAS NO EFFECT ON SEMAPHORE. 1 = ENABLED. WHEN EXTERNAL SIGNAL SPECIFIED BY S1 ExtSig Select IS ASSERTED HIGH FOR 1 CLOCK PERIOD, SEMAPHORE REGISTER S1 IN INCREMENTED.
S2 ExtSig Select	S2 EXTERNAL SIGNAL SELECT. SPECIFIES WHICH OF 8 EXTERNAL INPUT SIGNALS WILL GENERATE A SIGNAL TO UPDATE SEMAPHORE REGISTER. (SEE TABLE BELOW)
S2 SigEn	S2 EXTERNAL SIGNAL ENABLE. 0 = DISABLED. EXTERNAL SIGNAL HAS NO EFFECT ON SEMAPHORE. 1 = ENABLED. WHEN EXTERNAL SIGNAL SPECIFIED BY S2 ExtSig Select IS ASSERTED HIGH FOR 1 CLOCK PERIOD, SEMAPHORE REGISTER S2 IN INCREMENTED.
S3 ExtSig Select	S3 EXTERNAL SIGNAL SELECT. SPECIFIES WHICH OF 8 EXTERNAL INPUT SIGNALS WILL GENERATE A SIGNAL TO UPDATE SEMAPHORE REGISTER. (SEE TABLE BELOW)
S3 SigEn	S3 EXTERNAL SIGNAL ENABLE. 0 = DISABLED. EXTERNAL SIGNAL HAS NO EFFECT ON SEMAPHORE. 1 = ENABLED. WHEN EXTERNAL SIGNAL SPECIFIED BY S3 ExtSig Select IS ASSERTED HIGH FOR 1 CLOCK PERIOD, SEMAPHORE REGISTER S3 IN INCREMENTED.

FIG. 9G

991

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
																				E1 EVENTS								E0 EVENTS			
RESERVED								STU Re-start Sem	STU Re-start CC	CTU Re-start Sem	CTU Re-start CC	RSRVD								E1TPCWait	E1eot	E1STUeot	E1CTUeot	RSRVD				E0TPCWait	E0eot	E0STUeot	E0CTUeot

E0CTUeot	1 = TRIGGER E0 ACTION(S) WHEN CTUeot BECOMES TRUE (CTC:1→0)
E0STUeot	1 = TRIGGER E0 ACTION(S) WHEN STUeot BECOMES TRUE (STC:1→0)
E0TCzero	1 = TRIGGER E0 ACTION(S) WHEN BOTH CTC AND STC BECOME ZERO. (THE LATER COUNTER TO REACH ZERO TRIGGERS THE ACTION. IF THIS BIT IS SET, E0CTUeot AND E0STCeot ARE IGNORED.
E0TPCWait	1 = TRIGGER E0 ACTION(S) WHEN TPC BECOMES EQUAL WAITPC.
E0IncDreg	0 = NO POST-INCREMENT OF DREG 1 = POST-INCREMENT DREG IF IT IS A GENERAL REGISTER (GR0-GR3 ONLY)
E1CTUeot	1 = TRIGGER E1 ACTION(S) WHEN CTUeot BECOMES TRUE (CTC:1→0)
E1STUeot	1 = TRIGGER E1 ACTION(S) WHEN STUeot BECOMES TRUE (STS:1→0)
E1TCzero	1 = TRIGGER E1 ACTION(S) WHEN BOTH CTC AND STC BECOME ZERO.
E1TPCWait	1 = TRIGGER E1 ACTION(S) WHEN TPC BECOMES EQUAL WAITPC.
E1IncDreg	0 = NO POST-INCREMENT OF DREG 1 = POST-INCREMENT DREG IF IT IS A GENERAL REGISTER (GR0-GR3 ONLY)
CTU RestartCC	THIS FIELD SPECIFIES THE CONDITION WHICH, WHEN TRUE, CAUSES THE CTU TO RESTART AUTOMATICALLY (IF IT HOLD VALID TRANSFER PARAMETERS), AND UPDATES THE SEMAPHORE SPECIFIED BY CTURestartSem. 00 = DECREMENT 'CTURestartSem' WHEN CONDITION (Sem! = 0) BECOMES TRUE, AND INITIATE A CTU RESTART OPERATION. 01 = RESERVED 10 = RESERVED 11 = NO RESTART OPERATION
CTU RestartSem	SPECIFIES THE SEMAPHORE TO TEST FOR ZERO TO OBTAIN A TRUTH VALUE FOR CTURestartCC WHEN THE CTUWaitCC FIELD IS 00. 00 = S0 01 = S1 10 = S2 11 = S3
STU RestartCC	THIS FIELD SPECIFIES THE CONDITION WHICH, WHEN TRUE, CAUSES THE STU TO RESTART AUTOMATICALLY (IF IT HOLD VALID TRANSFER PARAMETERS), AND UPDATES THE SEMAPHORE SPECIFIED BY STURestartSem. 00=DECREMENT 'STURestartSem' WHEN CONDITION (Sem!=0) BECOMES TRUE AND INITIATE A STU RESTART OPERATION. 01 = RESERVED 10 = RESERVED 11 = NO RESTART OPERATION
STU RestartSem	SPECIFIES THE SEMAPHORE TO TEST FOR ZERO TO OBTAIN A TRUTH VALUE FOR STU RestartCC 00 = S0 01 = S1 10 = S2 11 = S3

FIG. 9H1

992

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SIGNAL Opcode						Sig mod		Cond Sem ID		Cond Sem Op		SCondition				Rsvd				Sem ID		Sem Op		Sig1	Sig0	Areg		Dreg			
IMMEDIATE ADDRESS (PRESENT ONLY WHEN Smod = x10, x11)																															
IMMEDIATE DATA (PRESENT ONLY WHEN Smod = x01, x11)																															

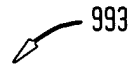
THE SIGNAL INSTRUCTION PROVIDES A MEANS FOR UPDATING A SEMAPHORE, ASSERTING INTERRUPT SIGNALS AND/OR SENDING A MESSAGE ON THE SCB SYNCHRONOUS WITH THE DMA INSTRUCTION STREAM.

Sogmod	00 = INDIRECT ADDRESS (ADDRESS IN REG 'Areg'), INDIRECT DATA (DATA IN REG 'Dreg') 01 = INDIRECT ADDRESS(ADDRESS IN REG 'Areg'), IMMEDIATE DATA (NEXT INST WORD) 10 = IMMEDIATE ADDRESS (NEXT INST WORD), INDIRECT DATA (DATA IN REG 'Dreg') 11 = IMMEDIATE ADDRESS (NEXT INST WORD),IMMEDIATE DATA (WORD FOLLOWING IMMEDIATE ADDRESS).
Cond SemID	SEMAPHORE ID. THIS SPECIFIES WHICH SEMAPHORE IS USED IN THE CONDITION COMPARISON. 00 = S0 01 = S1 10 = S2 11 = S3
Cond SemOp	SPECIFIES OPERATION TO PERFORM ON THE SEMAPHORE IF CONDITION IS TRUE. 00 = NO CHANGE TO SEMAPHORE 01 = DECREMENT THE SEMAPHORE BY 1 10 = INCREMENT THE SEMAPHORE BY 1 11 = CLEAR SEMAPHORE TO ZERO
SCondition	CONDITION WHICH, IF TRUE, ALLOWS THE SIGNAL TO OCCUR. SAME AS WAIT CONDITIONS, AND ASSUMES A COMPARISON WITH ZERO.
Sig0	1 = ASSERT INTERRUPT SIGNAL 0 HIGH FOR TWO CLOCK CYCLES, THEN LOW. 0 = DO NOT ASSERT.
Sig1	1 = ASSERT INTERRUPT SIGNAL 1 HIGH FOR TWO CLOCK CYCLES, THEN LOW. 0 = DO NOT ASSERT
Areg	WHEN Sigmod = 00 OR Sigmod = 01, SPECIFIES AN INTERNAL REGISTER (GR0-GR3) WHOSE CONTENTS SPECIFY AN ADDRESS ON THE SYSTEM CONTROL BUS TO WHICH DATA IS TO BE SENT. NOT USED IF Dreg = '1111'

FIG. 9H2

Dreg	WHEN Sigmod = 00 OR Sigmod = 10 (INDIRECT DATA), THIS FIELD SPECIFIES THE REGISTER TO BE SENT AS DATA ON THE SYSTEM CONTROL BUS. IF THIS FIELD CONTAINS '1111', THEN NO MESSAGE IS SENT REGARDLESS OF THE VALUE OF Sigmod. THE FOLLOWING REGISTER ASSIGNMENTS INDICATE THAT SEVERAL INTERNAL REGISTERS MAY BE USED AS MESSAGE DATA, INCLUDING GRx REGISTERS, TSR (STATUS) REGISTERS, TPC REGISTER AND THE SEM (SEMAPHORE) REGISTER.
	0000-GR0
	0001-GR1
	0010-GR2
	0011-GR3
	1000-TSR0
	1001-TSR1
	1010-TSR2
	1011-TSR3
	1100-TPC
	1101-SEM
	1111-DO NOT SEND MESSAGE
Sem ID	SPECIFIES A SEMAPHORE TO UPDATE WHEN SIGNAL IS PERFORMED. 00 = SEMAPHORE 0 01 = SEMAPHORE 1 10 = SEMAPHORE 2 11 = SEMAPHORE 3
Sem Op	00 = NO CHANGE TO SEMAPHORE 01 = DECREMENT THE SEMAPHORE BY 1 10 = INCREMENT THE SEMAPHORE BY 1 11 = CLEAR SEMAPHORE TO ZERO

FIG. 9I1



31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
E1 ACTIONS																E0 ACTIONS															

E1 S3 Op	E1 S2 Op	E1 S1 Op	E1 S0 Op	E0Sig1	E0Sig0	E1 Areg	E1 Dreg	E0 S3 Op	E0 S2 Op	E0 S1 Op	E0 S0 Op	E0Sig1	E0Sig0	E0 Areg	E0 Dreg

E0 Dreg	SPECIFIES A REGISTER TO BE SENT (IF NOT '1111') AS MESSAGE DATA WHEN E0 EVENT OCCURS.
	0000-GR0
	0001-GR1
	0010-GR2
	0011-GR3
	1000-TSR0
	1001-TSR1
	1010-TSR2
	1011-TSR3
	1100-TPC
	1101-SEM
	1111-DO NOT SEND MESSAGE
E0 Areg	SPECIFIES A REGISTER WHICH PROVIDES THE MESSAGE ADDRESS WHEN E0 EVENT OCCURS.
	00-GR0
	01-GR1
	10-GR2
	11-GR3
E0Sig0	0 = DO NOT ASSERT INTERRUPT SIGNAL 0. 1 = ASSERT INTERRUPT SIGNAL 0 ACTIVE 1 FOR 2 CYCLES WHEN E0 EVENT OCCURS
E0Sig1	0 = DO NOT ASSERT INTERRUPT SIGNAL 1. 1 = ASSERT INTERRUPT SIGNAL 1 ACTIVE 1 FOR 2 CYCLES WHEN E0 EVENT OCCURS
E0 S0-S3 Op	EACH 2-BIT FIELD SPECIFIES THE ACTION WHEN E0 EVENT OCCURS, ONE FIELD PER SEMAPHORE: 00 = NO CHANGE TO SEMAPHORE 01 = DECREMENT THE SEMAPHORE BY 1 10 = INCREMENT THE SEMAPHORE BY 1 11 = CLEAR SEMAPHORE TO ZERO
E1 Dreg	SPECIFIES A REGISTER TO BE SENT (IF NOT '1111') AS MESSAGE DATA WHEN E1 EVENT OCCURS.
	0000-GR0
	0001-GR1
	0010-GR2
	0011-GR3
	1000-TSR0
	1001-TSR1
	1010-TSR2
	1011-TSR3
	1100-TPC
	1101-SEM
	1111-DO NOT SEND MESSAGE

FIG. 9I2

E1 Areg	SPECIFIES A REGISTER WHICH PROVIDES THE MESSAGE ADDRESS WHEN E1 EVENT OCCURS.
	00-GR0
	01-GR1
	10-GR2
	11-GR3
E1Sig0	0 = DO NOT ASSERT INTERRUPT SIGNAL 0. 1 = ASSERT INTERRUPT SIGNAL 0 ACTIVE 1 FOR 2 CYCLES WHEN E1 EVENT OCCURS.
E1Sig1	0 = DO NOT ASSERT INTERRUPT SIGNAL 1. 1=ASSERT INTERRUPT SIGNAL 1 ACTIVE 1 FOR 2 CYCLES WHEN E1 EVENT OCCURS.
E0 S0-S3 Op	EACH 2-BIT FIELD SPECIFIES THE ACTION WHEN E1 EVENT OCCURS, ONE FIELD PER SEMAPHORE: 00 = NO CHANGE TO SEMAPHORE 01 = DECREMENT THE SEMAPHORE 10 = INCREMENT THE SEMAPHORE BY 1 11 = CLEAR SEMAPHORE TO ZERO

FIG. 9J

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
GRx (x=0,1,2,3,...)																															
THE GENERAL (MESSAGE) REGISTERS GR0, GR1, GR2, AND GR3 ARE USED TO STORE ADDRESSES AND DATA FOR SENDING CONTROL MESSAGES TO SCB DEVICES. THEY MAY BE LOADED USING THE LIMGR INSTRUCTION, OR BY DIRECT WRITE BY AN SCB BUS MASTER.																															

FIG. 10A

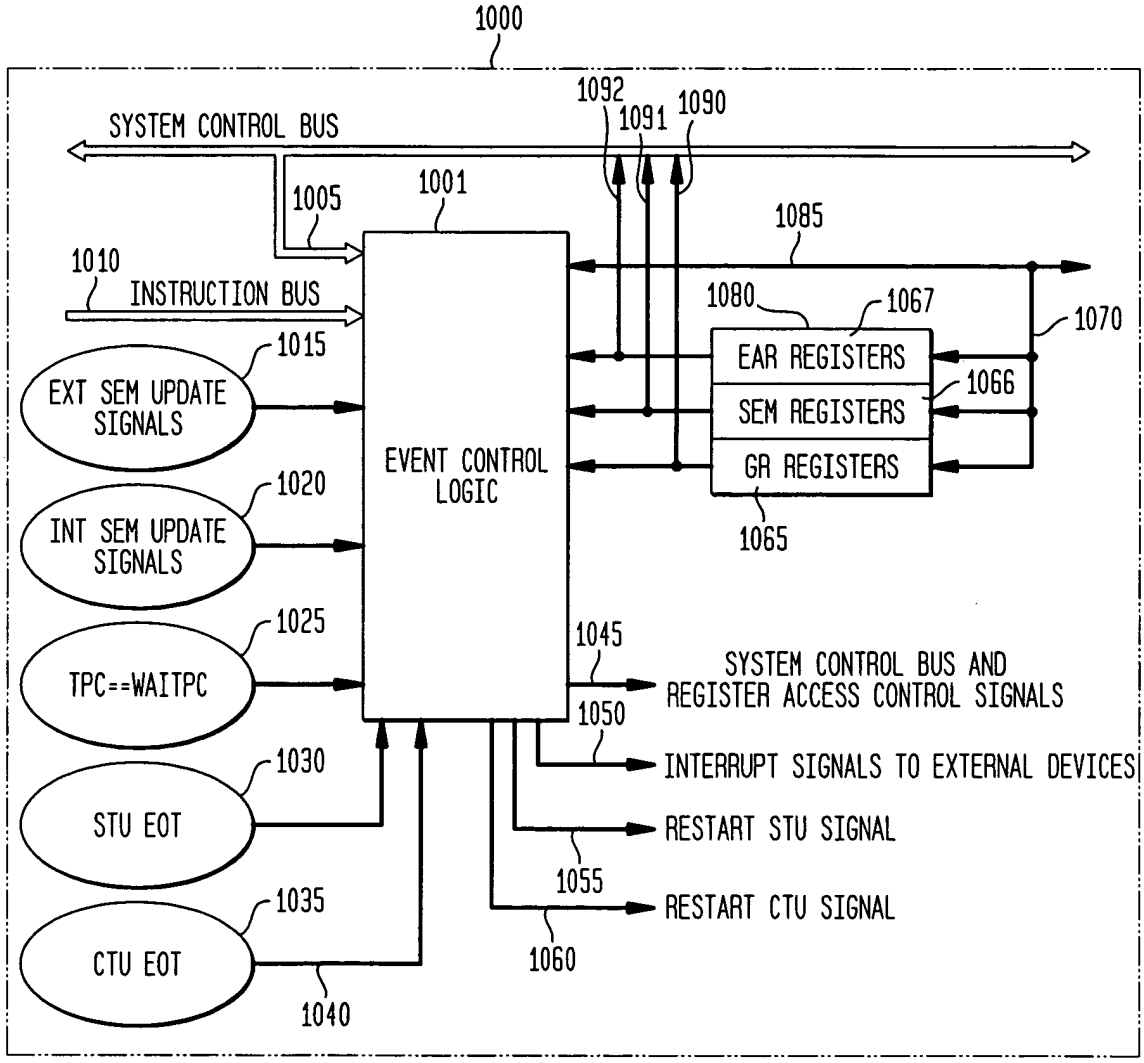

1000
SYSTEM CONTROL BUS
1092
1091
1090
1005
1001
1085
1010
INSTRUCTION BUS
1080
1067
1070
EAR REGISTERS
1066
SEM REGISTERS
GR REGISTERS
1065
1015
EXT SEM UPDATE SIGNALS
EVENT CONTROL LOGIC
1020
INT SEM UPDATE SIGNALS
1025
TPC==WAITPC
1045
SYSTEM CONTROL BUS AND REGISTER ACCESS CONTROL SIGNALS
1050
INTERRUPT SIGNALS TO EXTERNAL DEVICES
1030
STU EOT
RESTART STU SIGNAL
1055
1035
CTU EOT
RESTART CTU SIGNAL
1060
1040

FIG. 10B

1082

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
WAIT Opcode								Sem ID		Sem Op		SCondition				NOT USED								Compare Val							

THE WAIT INSTRUCTION CAUSES INSTRUCTION FETCHING TO STOP WHILE THE SPECIFIED WAIT CONDITION IS TRUE. THE WAIT CONDITION IS SPECIFIED BY THE RELATIONSHIP BETWEEN A SPECIFIED SEMAPHORE (S0, S1, S2 OR S3), AND AN 8-BIT IMMEDIATE VALUE SPECIFIED IN THE INSTRUCTION. THE IMMEDIATE VALUE IS SUBTRACTED FROM THE SEMAPHORE AND THE FLAGS ARE SET TO ESTABLISH THEIR RELATIONSHIP. THE CONDITIONS ALLOW THE VALUES TO BE INTERPRETED AS EITHER SIGNED OR UNSIGNED NUMBERS. WHEN THE CONDITION SPECIFIED IS (OR BECOMES) FALSE, THE SPECIFIED SEMAPHORE IS UPDATED ACCORDING TO THE UPDATE CONTROL FIELD (BITS [21:20]).

SemID	SEMAPHORE ID. THIS SPECIFIES WHICH SEMAPHORE IS USED IN THE CONDITION COMPARISON. 00 = S0 01 = S1 10 = S2 11 = S3
SCondition	SEMAPHORE CONDITION. 0000 = ALWAYS (WAIT UNTIL EXPLICIT COMMAND CAUSES A PROCESSING STATE CHANGE) 0001 = EQUAL 0010 = NOT EQUAL 0011 = HIGHER THAN 0100 = HIGHER THAN OR EQUAL 0101 = LOWER THAN 0110 = LOWER THAN OR EQUAL 0111 = CTUeot 1000 = STUeot 1001 = !ICTUeot (CTC NOT ZERO) 1010 = !ISTUeot (STC NOT ZERO) 1011 = GREATER THAN OR EQUAL 1100 = GREATER THAN 1101 = LESS THAN OR EQUAL 1110 = LESS THAN 1111 = RESERVED
SemOp	00 = NO CHANGE TO SEMAPHORE WHEN WAIT CONDITION IS/BECOMES FALSE 01 = DECREMENT SEMAPHORE BY 1 WHEN WAIT CONDITION IS/BECOMES FALSE 10 = INCREMENT SEMAPHORE BY 1 WHEN THE WAIT CONDITION IS/BECOMES FALSE 11 = CLEAR TO ZERO WHEN THE WAIT CONDITION IS/BECOMES FALSE
Compare Val	IMMEDIATE 8-BIT VALUE WHICH IS SUBTRACTED FROM THE SPECIFIED SEMAPHORE VALUE TO OBTAIN THE COMPARISON CONDITIONS.

FIG. 10C

1083

SYSTEM BUFFER IS 1K WORDS, SPLIT INTO 4 256 WORD BUFFERS. THE PRODUCER TASK IS GENERATING DATA INTO THESE BUFFERS IN A CIRCULAR FASHION. THE CONSUMER TASK (ON THE DSP) HAS ONLY A 256 WORD BUFFER, SPLIT INTO 4x64 WORD BLOCKS. EVERY TIME THE PRODUCER TASK FINISHES FILLING A BUFFER IT SIGNALS SEMAPHORE S1 BY WRITING TO THE APPROPRIATE COMMAND ADDRESS ON THE SCB. THE LIMEAR INSTRUCTION HAS CONFIGURED THE TRANSFER CONTROLLER TO RESTART THE STU ANYTIME IT IS IDLE AND S1 IS NON-ZERO, SINCE THE CTU HAS A NON-ZERO TRANSFER COUNT, IT ENTERS THE TRANSFER STATE AND 64 WORDS OF DATA ARE MOVED TO THE CONSUMER TASK BUFFER (THE MINIMUM OF 256 AND 64).	

linear STUrestart=s1, CTUrestart=s0,
E0=STUeot, A0=assert(0), E1=CTUeot,
A1=(msgaddr=mbox1, msdata=GR0),
	LIMEAR instruction:
	IF S1 NOT ZERO AT STU EOT THEN
	DECREMENT S1 AND RESTART STU.
	IF S0 NOT ZERO AR CTU EOT THEN
	DECREMENT S0 AND RESTART CTU.
	AT STU EOT ASSERT SIGNAL 0.
	AT CTU EOT SEND CONTENTS OF GR0 TO SCB
	ADDRESS "mbox1".

tsi.circular tc = 256, addr = 0x12000000 bufinit = 0, bufsize = 1024;	LOAD STU FOR INBOUND TRANSFER OF 256 WORDS WITHIN A CIRCULAR BUFFER OF 1K WORDS.
tsi.circular tc = 64, addr = 0x00200300, bufinit = 0, bufsize = 256;	LOAD CTU FOR INBOUND TRANSFER OF 64 WORDS WITHIN A CIRCULAR BUFFER OF 256 WORDS.
wait;	WAIT UNTIL A PROCESSOR WRITES A RESUME COMMAND.